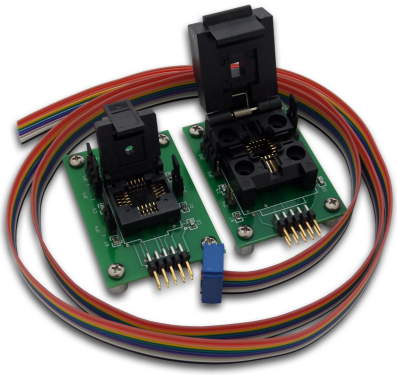
MODEL EB-L & EB-J ANALOG SURFACE MOUNT ACCELEROMETER TEST SET



- Easily test SDI's analog surface mount accelerometers during concept design or prior to installation
- Chips can be removed and remain unharmed
- Fully assembled for immediate implementation
- Compatible with SDI Models 1510, 1521, and 1531
- Ideal to use with the SDI Model 3330 or 3340 G-Loggers
- Configurations available for SDI's JLCC or LCC chip packages
- Contents include:
  - One test board with L or J package zero-insertion force test socket and compatible jumpers installed
  - One Ribbon cable with 10-pin connector

The Model EB-L Analog and EB-J Analog Test Sets provide a convenient means of testing and evaluating SDI Models 1510, 1521, and 1531 surface mount accelerometers in either the LCC or JLCC package format. The zero-insertion-force socket is pre-fitted to the board, which includes set jumpers for advanced features of SDI accelerometers. A 10-pin connector and ribbon cable is provides connections to the user's test equipment. The EB-L Set, EB-J Set, and SDI Surface Mount Accelerometers are each sold separately.

OPERATION

The EB-J and EB-L Analog Test Sets come fully assembled and ready to integrate with a test system.

1. Install the accelerometer into the socket with pin 1 (▶) towards the socket hinge.
2. With the 10 pin connector on the left (see board layout below) jumper pins are 1-2-3
   a. EB-L Analog has 2 pin jumpers for both JP4 and JP5.
   b. EB-J Analog has a 2 pin jumper for only JP4 . There is no JP5 on this board

Please see specific 1510, 1521, 1525, and 1531 accelerometer data sheets for a complete description of functions.

SIGNALS & CABLE SPECIFICATIONS

PIN #	SIGNAL NAME	SIGNAL DESCRIPTION	WIRE COLOR
1	DV	Deflection voltage input	Brown wire *
2	Clk Out	Master CLK OUT (NA for 1510) Set JP2	Red wire
3	I_T/ CLK IN	Temperature output/ Slave CLK IN (NA for 1510) Set JP1 and JP4 **	Pink wire
4	VR	+5 volt Reference Voltage input . Set JP3 to use ext source.	Yellow wire
5	AOP	Analog output, Positive	Green wire
6	VDD	+5V Power	Blue wire
7	-	(not used)	Purple wire
8	AON	Analog output, Negative	Grey wire
9	+2.5V	+2.5V Reference	White wire
10	GND	Ground	Black wire

* PIN 1 is marked on header cable with a triangle ▶
**PIN 3 is dual function configure with JP1, JP2 and JP4 jumpers.

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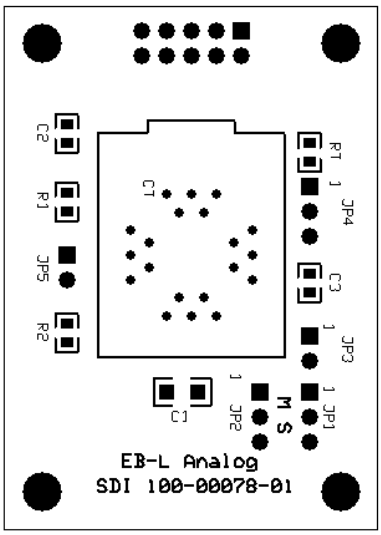
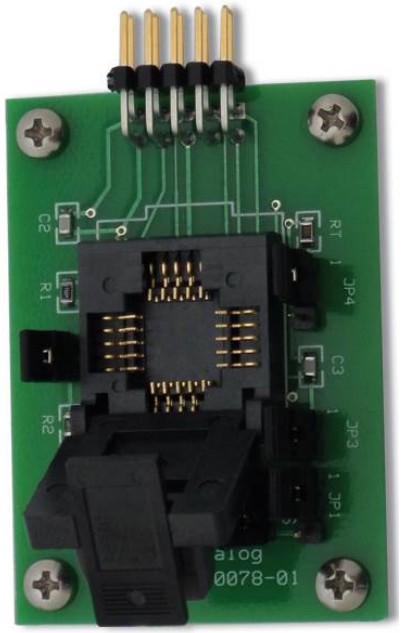
EB-L ANALOG BOARD JUMPER DESCRIPTIONS

Default settings in **BOLD.**

JP	1-2	2-3	NO JUMPER	COMMENTS
1	Slave clock	**Internal CLK**	NA	Int/Ext CLK setting.
2	Master CLK OUT ON	**Master CLK OUT OFF**	NA	CLK OUT
3	VR and 2.5 volt from VDD	**NA**	External VR	Separate VR and VDD
4	**Temp signal circuit**	1510L setting only.	CLK IN at PIN 3	Dual function
5	**2.5 volt from VR**	NA	External 2.5 volt	2.5 volts at pin 9





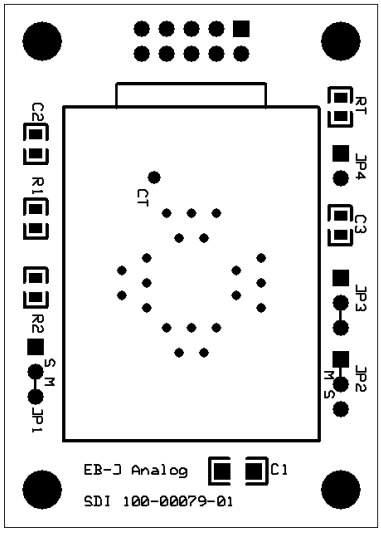
ADDITIONAL NOTES: EB-L ANALOG JUMPER USE

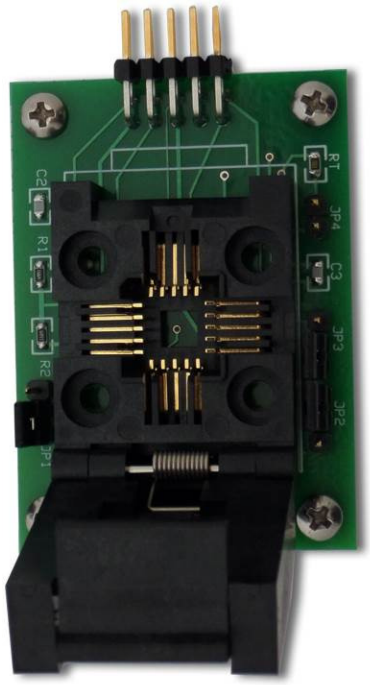
1. Slave mode, SDI 1521, 1525 and 1531 LCC accelerometers may be configured to run from an external CLK, to keep them synchronized with other external components. JP 1 set to 1-2 turns off both the internal clock and temperature output signal.
2. Master mode. Alternative option in a multiple axis configuration is to configure one of the accelerometers to provide a clock to the other Slave accelerometers (and external components if desired). JP 2 set to 1-2 turns on the CLK OUT from the designated Master accelerometer.
3. If JP 3 is installed, VR draws power from VDD. Similarly, with JP 5 installed the 2.5 volt is also derived from VR. Remove JP 3 to provide external 5 volts to VR at pin 4 and JP 5 to provide external 2.5 volts at pin 9.
4. The 1521 and 1531 have a temp signal output capability when in default mode or Master mode. The voltage is approximately 1 - 1.3 volts at room temperature. Set JP 4 to 1-2. When SDI 1521 and 1531 are in Slave mode (see note 1 above) the temperature output signal is disabled. Omitting JP 4 completely removes the resistor used in the temperature circuit or the recommended pull up line for 1510. A CLK may then be provided at PIN 3 to the accelerometer.
5. The 1510 is only available as an LCC and has no temperature output signal or ability to configure Master/ Slave. Use default jumper settings except for JP4 to 2-3.

EB-J ANALOG BOARD JUMPER DESCRIPTIONS

Default settings in **BOLD.**

JP	1-2	2-3	NO JUMPER	COMMENTS
1	Slave clock	**Internal CLK**	NA	Int/Ext CLK setting.
2	Master CLK OUT ON	**Master CLK OUT OFF**	NA	CLK OUT
3	External VR and 2.5 volt	**VR 5 +2.5 volt derived from VDD**	NA	Separate VR and VDD
4	**Temp signal circuit**	NA	CLK IN at PIN 3	Dual function





ADDITIONAL NOTES: EB-J ANALOG JUMPER USE

1. Slave mode, SDI 1521, 1525 and 1531 JLCC accelerometers may be configured to run from an external CLK, to keep them synchronized with other external components. JP 1 set to 1-2 turns off both the internal clock and temperature output signal.
2. Master mode. Alternative option in a multiple axis configuration is to configure one of the accelerometers to provide a clock to the other Slave accelerometers (and external components if desired). JP 2 set to 1-2 turns on the CLK OUT from the designated Master accelerometer.
3. If JP 3 2-3 is installed , VR draws power from VDD. Move JP 3 to 1-2 and provide external 5 volts to VR at pin 4.
4. The 1521-1531 have a temp signal output capability when in default mode or Master mode. The voltage is approximately 1 - 1.3 volts at room temperature. Set JP 4 to 1-2. When SDI 1521-1531 are in Slave mode (see note 1 above) the temperature output signal is disabled. Omitting JP 4 completely removes the resistor used in the temperature circuit. A CLK may then be provided at PIN 3 to the accelerometer.